

Docket No.: 0941-0872P

Application No. 10/724,201
Amendment dated November 23, 2005
Reply to Office Action of August 23, 2005

AMENDMENTS TO THE CLAIMS

1. (Withdrawn) A method of reducing the pattern effect in the CMP process, comprising the steps of:

- (a) providing a semiconductor substrate having a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;
- (b) performing a first CMP process to remove part of the conductive layer before the barrier layer is polished, thereby a step height of the conductive layer is reduced;
- (c) depositing a layer of material substantially the same as the conductive layer over the conductive layer; and
- (d) performing a second CMP process to expose the patterned dielectric layer.

2. (Withdrawn) The method as claimed in claim 1, wherein the conductive layer comprises copper or copper alloy.

3. (Withdrawn) The method as claimed in claim 1, wherein the patterned dielectric layer comprises silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate glass.

4. (Withdrawn) The method as claimed in claim 1, wherein the barrier layer comprises Ta, Ti, TaN, TiN, or WN.

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5. (Withdrawn) The method as claimed in claim 2, wherein the deposition of copper or copper alloy is performed using electroplating, CVD, or PVD.

6. (Withdrawn) The method as claimed in claim 1, wherein the top surface of the remaining conductive layer after performing the first CMP process is higher than the barrier layer by more than 10Å.

7. (Withdrawn) The method as claimed in claim 6, wherein the top surface of the remaining conductive layer after performing the first CMP process is higher than the barrier layer by from 100Å to 1000Å.

8. (Withdrawn) The method as claimed in claim 1, wherein the top surface of the remaining conductive layer after performing the first CMP process is approximately planar.

9. (Withdrawn) A method of eliminating dishing phenomena after a CMP process, comprising the steps of:

providing a semiconductor substrate having a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;

performing a first CMP process to an end point of polishing to remove part of the conductive layer, wherein the dishing phenomena occur on the conductive layer;

depositing a layer of material substantially the same as the conductive layer over the conductive layer; and

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performing a second CMP process to expose the patterned dielectric layer.

10. (Withdrawn) The method as claimed in claim 9, wherein the conductive layer comprises copper or copper alloy.

11. (Withdrawn) The method as claimed in claim 9, wherein the dielectric layer comprises silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate glass.

12. (Withdrawn) The method as claimed in claim 9, wherein the barrier layer comprises Ta, Ti, TaN, TiN, or WN.

13. (Withdrawn) The method as claimed in claim 10, wherein the deposition of copper or copper alloy is performed using electroplating, CVD, or PVD.

14. (Withdrawn) The method as claimed in claim 9, wherein the top surface of the layer deposited in the step of depositing a layer of material substantially the same as the conductive layer over the conductive layer is higher than the barrier layer.

15. (Currently Amended) A CMP rework method, comprising the steps of:
providing a semiconductor substrate which has a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;

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performing a first CMP process to remove part of the conductive layer;
depositing a layer of material with a planar surface substantially the same as the
conductive layer over the conductive layer; and
performing a second CMP process to expose the patterned dielectric layer.

16. (Original) The method as claimed in claim 15, wherein the conductive layer
comprises copper or copper alloy

17. (Original) The method as claimed in claim 15, wherein the dielectric layer comprises
silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate
glass

18. (Original) The method as claimed in claim 15, wherein the barrier layer comprises
Ta, Ti, TaN, TiN, or WN.

19. (Original) The method as claimed in claim 16, wherein the deposition of copper or
copper alloy is performed using electroplating, CVD, or PVD.

20. (Currently Amended) The method as claimed in claim 15, wherein the top surface of
the layer deposited in said the step of depositing said a layer of material substantially the same as
the conductive layer over the conductive layer is higher than the barrier layer.

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21. (Currently Amended) The method as claimed in claim 15, wherein the semiconductor substrate is reported by a CMP machine as an abnormally polished wafer at a predetermined CMP end point after performing said a first CMP process to remove part of the conductive layer.

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